

Claims

1. A digital amplifier including a noise shaper and a dither generator arranged to
5 introduce noise to the shaper, said generator using a seed value derived from
a state variable of said shaper.

2. A digital amplifier as claimed in claim 1 and wherein the number of bits in the
generated noise exceeds that of the seed value.

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3. A digital amplifier as claimed in Claim 1 or Claim 2 and wherein the dither
generator includes shift registers of predetermined bit lengths to receive said
seed values and provide a noise output.

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4. A digital amplifier as claimed in any preceding claim including means for
scaling said noise.

5. A digital amplifier including a clocked modulator wherein clock activity is
monitored by counting divided multiples of the clock.

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6. A digital amplifier as claimed in claim 5 and including multiple clocks and
wherein a first clock is used to count a second clock.

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7. A digital amplifier as claimed in claim 6 and wherein a divided multiple of said
second clock is counted.

8. A digital amplifier as claimed in any of claims 5 to 7 and wherein output is
disabled when a clocking error is detected.

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9. A digital amplifier as claimed in any of claims 5 to 8 and wherein when a
clocking error is detected, a parameter indicative of the error is stored.

10. A digital amplifier having a detection arrangement to provide an error signal when there is no modulator drive or clock loss or undefined input states to an h-bridge leg.

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11. A digital amplifier having a deadtime generation or control arrangement substantially as herein described.

12. A digital amplifier in which deadtime is balanced on rising and falling edges of
10 signals.

13. A digital amplifier in which deadtime is adaptive to gate charge of the output switching device.

15 14. A digital amplifier in which deadtime is temperature independent or temperature compensated.

15. A digital amplifier having programmable deadtime control or inter-channel delay or ABD delay which may be optimized by means of programming
20 registers.

16. A digital amplifier as claimed in claim 15 and wherein deadtime is controlled by a resistor or programming register.

25 17. A digital amplifier substantially as herein described.

18. The features hereof in any novel or inventive combination.

19. A digital amplifier including means for reducing the effect of peak or spike
30 voltages from the power supply.

20. A digital amplifier as claimed in claim 19 and wherein said means comprises a clamp diode in association with power supply filtering.

21. An integrated half bridge device laid out substantially as herein described.

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22. An integrated half bridge device with pin out substantially as herein described or equivalent thereto.

23. A digital amplifier having high side over current protection substantially as
10 herein described.

24. A digital amplifier in which the layout and design of the reclocker substantially
herein described.